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DATA REALIGNMENT TECHNIQUES FOR SERIAL-TO-PARALLEL CONVERSION

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 10/269,370 filed October 10, 2002 (Attorney Docket No. 015114-063100US), which is incorporated by reference herein. is now a U.S. Patent 6,707,399

BACKGROUND OF THE INVENTION

[0002] The present invention relates to data realignment in serial-to-parallel converters, and more particularly, to techniques for realigning the boundary between data bytes when converting serial data to parallel data.

[0003] A serial-to-parallel converter circuit is used to convert a serial data stream into a parallel data stream. Bits of data are shifted into a shift register from a single input data stream. The data bits stored in the register are then simultaneously shifted out of the register along parallel signal lines as parallel data. Each data bit is output on a separate parallel signal line. The data bits are shifted out of the register as bytes of data (e.g., 8 bits each). Thus, the registers groups serial data bits into data bytes on parallel signal lines.

[0004] The register determines the boundary between one data byte and the next data byte. Typically, when serial data is converting to parallel data, the boundary between data bytes is determined randomly, depending upon when the data transmitting and receiving devices power up.

[0005] Therefore, it would be desirable to provide techniques to realign the boundary between output data bytes from a serial-to-parallel data converter to match a preset data boundary.

BRIEF SUMMARY OF THE INVENTION

[0006] The present invention includes techniques for adjusting the boundary between bytes of data in a serial-to-parallel converter. Bits of serial data are shifted into a first register. A first clock signal controls the shifting of data into the first register. Data bytes are then shifted out of